32. (New) The apparatus of claim 30, wherein:

the address translator comprises a graphics translation lookaside buffer.

REMARKS

Claims 1-29 have been rejected under 35 USC 102(e) as being anticipated by U.S. patent no. 6,282,625 ("Porterfield"). Applicants respectfully traverse these rejections in view of the amendment because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Independent claims 8, 15, 23 and 30, as well as dependent claim 22, each recite that the translated address has more bits than the address before translation. Porterfield does not disclose this limitation, and in fact does not try to compare the size of the translated address to the size of the pre-translation address.

Independent claim 30 recites a separate interface to each of the graphics controller and the bus controller. Porterfield does not disclose separate interfaces to these two devices.

Further, independent claims 8, 19, as well as dependent claims 17, 29, 31 each recite that the same translation table is used to translate addresses from a bus controller and to translate addresses from a graphics controller. Porterfield does not disclose using the same translation device to translate addresses from both a graphics controller and a bus controller.

Each of the pending dependent claims depends from one of the above-mentioned independent claims, and therefore contains the same limitations not disclosed by Porterfield.

Claims 1-7, 10 and 11 have been cancelled, rendering the rejection of these claims moot.

New claims 30-32 have been added. Support for these claims may be found in Figs. 3, 4 and the supporting text in the specification.

Several minor changes have been made in various claims to correct antecedent problems and to more consistently refer to bus-controller related items as 'first' and to graphics-controller related items as 'second'. These changes are not substantive.

CONCLUSION

For the foregoing reasons, Applicant submits that claims 8-9 and 12-31 are now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned at the telephone number shown below as soon as possible. No fee is believed due in connection with this response. If this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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APPENDIX A

Marked-up version of amended claims, and new claims

1-8. (Cancelled)

8. (Amended once) A method, comprising:

using a conversion table to translate a first address from a graphics controller to a second address to a memory; and

using the conversion table to translate a [second] third address from a bus controller to a fourth address to the memory;

wherein the second address has a greater number of bits than the first address and the fourth address has a greater number of bits than the third address .

9. (Amended once) The method of claim 8, wherein said using the conversion table to translate the third address includes using a translation lookaside buffer.

10-11. (Cancelled)

12. (Amended once) The method of claim 8, wherein said using the conversion table to translate the [second] third address includes:

comparing a first portion of the [second] third address with entries in a first table;

if the first portion matches a particular one of the entries in the first table,

combining a value associated with the particular one with a second portion of the [second] third address to form [a translated] the fourth address.

13. (Amended once) The method of claim 12, further comprising:

if the first portion does not match any of the entries in the first table, referring to a second table to translate the [second] third address.

14. (Amended once) The method of claim 13, wherein:

said comparing includes comparing the first portion of the [second] third address with entries in [a] the first table in an input-output controller; and

said referring to the second table includes referring to the second table in main memory.

15. (Amended once) An apparatus, comprising:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of an initial address in the input register with entries in the translation lookaside buffer; and if a matching entry is found, to combine a first value associated with the matching entry with a second portion of the initial address to form a first

translated address and hold the first translated address in the output register;

wherein the first value has a greater number of bits than the first portion .

17. (Amended once) The apparatus of claim 16, wherein:

the control logic includes logic for first and second control flows;

the [first] second control flow is to translate an initial graphics controller address and does not access the second table; and

the [second] first control flow is to translate an initial bus controller address and [can] access the second table.

19. (Amended once) A system, including:

a processor;

a memory;

a graphics controller;

a bus controller;

an input-output controller coupled to the processor, memory, graphics controller and bus controller, the input-output controller including:

a translation lookaside buffer coupled to an input register and an output register;

control logic coupled to the translation lookaside buffer, the input register, and the output register;

wherein the control logic is to compare a first portion of [an] a first initial address from the bus controller in the input register with entries in the translation lookaside buffer; and if a first matching entry is found, to combine a first value associated with the first matching entry with a second portion of the first initial address to form a first translated address and hold the first translated address in the output register;

wherein the control logic is further to compare a first portion of a second initial address from the graphics controller in the input register with the entries in the translation lookaside buffer; and if a second matching entry is found, to combine a second value associated with the second matching entry with a second portion of the second initial address to form a second translated address and hold the second translated address in the output register.

20. (Amended once) The system of claim 19, wherein the control logic is further to:

access a table in memory if the first matching entry is not found;

find a [second] third value in the table associated with the first portion of the first initial address;

combine the [second] third value with the second portion of the first initial adress to form a [second] third translated address: and

hold the [second] third translated address in the output register.

21. (Amended once) The system of claim 20, wherein:

the control logic includes logic for first and second control flows;

the [first] second control flow is to translate an initial graphics controller address and does not access the [second] table; and

the [second] first control flow is to translate an initial bus controller address and [can] access the [second] table.

22. (Amended once) The system of claim 20, wherein the first [and second] translated address[es each have] has more bits than the first initial address and the second translated address has more bits than the second initial address .

23. (Amended once) A machine-readable medium having stored thereon instructions, which when executed by a machine cause said processor to perform:

reading a first address containing a first number of bits and having an upper portion and a lower portion;

comparing the upper portion with a plurality of first entries in a first table;

if the upper portion matches a particular one of the plurality of first entries:

selecting a second entry in the first table associated with the particular one of the plurality of first entries;

combining the second entry with the lower portion to form a first translated address; and

transmitting the first translated address;

wherein the second entry contains a greater number of bits than the upper portion.

26. (Amended once) The medium of claim 24, wherein said transmitting the first [and second] translated address[es] includes transmitting to a memory controller.

28. (Amended once) The medium of claim 23, wherein said reading [providing] a first address includes reading [providing] a first address from a bus controller.

30. (New) An apparatus comprising:

an address translator having a first interface to couple to a memory controller, a second interface to couple to a graphics controller, a third interface to couple to a bus controller, and a table of entries, each entry having a first portion and a second portion;

a translation control circuit coupled to the address translator to program the entries in the address translator;

wherein the address translator is to translate an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface.

31. (New) The apparatus of claim 30, wherein:

the address translator is further to translate an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface.

32. (New) The apparatus of claim 30, wherein:

the address translator comprises a graphics translation lookaside buffer.